In The Claims:

Claims 1-74 (canceled)

75. (new) A multi-chip structure comprising:

a first chip;

a second chip;

a conductive pillar on the first chip, wherein said conductive pillar has a height greater than 3 microns; and

a tin-containing material connecting said conductive pillar to said second chip.

76. (new) The structure of Claim 75, wherein said conductive pillar comprises copper.

77. (new) The structure of Claim 75, wherein said conductive pillar comprises nickel.

78. (new) The structure of Claim 75, wherein said conductive pillar comprises gold.

79. (new) The structure of Claim 75, wherein said conductive pillar comprises tin.

80. (new) The structure of Claim 75 further comprising a wire formed by a wirebonding process and connected to said first chip.

81. (new) The structure of Claim 75, wherein said tin-containing material further comprises lead.

82. (new) The structure of Claim 75, wherein said tin-containing material further comprises silver.

83. (new) A multi-chip structure, comprising:

a first chip comprising:

a semiconductor substrate comprising multiple MOS devices,

an interconnection layer over said semiconductor substrate,

a first pad over said semiconductor substrate, a passivation layer over said interconnection layer, an opening in said passivation layer exposing said first pad, and

a second pad over said passivation layer, wherein said second pad is connected to said first pad and has a position different from that of said first pad from a top view;

a conductive pillar on said second pad, wherein said conductive pillar has a height greater than 3 microns;

a second chip over said first chip; and

a tin-containing material connecting said conductive pillar to said second chip.

84. (new) The structure of Claim 83, wherein said conductive pillar comprises copper.

85. (new) The structure of Claim 83, wherein said conductive pillar comprises nickel.

86. (new) The structure of Claim 83, wherein said conductive pillar comprises gold.

87. (new) The structure of Claim 83, wherein said conductive pillar comprises tin.

88. (new) The structure of Claim 83, wherein said second pad comprises gold.

89. (new) The structure of Claim 83, wherein said second pad comprises an electroplated metal.

90. (new) The structure of Claim 83, wherein said second has a thickness greater than 1 micron.

91. (new) The structure of Claim 83 further comprising a wire formed by a wirebonding process and connected to said first chip.

92. (new) The structure of Claim 83, wherein said tin-containing material further comprises lead.

93. (new) The structure of Claim 83, wherein said tin-containing material further comprises silver.

94. (new) A multi-chip structure, comprising:

a first chip comprising:

a semiconductor substrate comprising multiple MOS devices,

an interconnection layer over said semiconductor substrate,

a first pad over said semiconductor substrate, a passivation layer over said interconnection layer, an opening in said passivation layer exposing said first pad,

a trace over said passivation layer, and

a second pad over said passivation layer, wherein said second pad is connected to said first pad through said trace and has a position different from that of said first pad from a top view;

a second chip over said first chip; and

a bump connecting said second pad to said second chip.

95. (new) The structure of Claim 94, wherein said bump comprises copper.

96. (new) The structure of Claim 94, wherein said bump comprises nickel.

97. (new) The structure of Claim 94, wherein said bump comprises gold.

98. (new) The structure of Claim 94, wherein said bump comprises tin.

99. (new) The structure of Claim 94, wherein said bump comprises lead.

100. (new) The structure of Claim 94, wherein said bump comprises silver.

101. (new) The structure of Claim 94 further comprising a wire formed by a wirebonding process and connected to said first chip.